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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/294,341	04/20/1999	MASAAKI HIROKI	0756-1964	6027

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EXAMINER	
LIANG, REGINA	
ART UNIT	**PAPER NUMBER**
2629	

DATE MAILED: 06/26/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/294,341	HIROKI, MASAAKI	
	Examiner	Art Unit	
	Regina Liang	2629	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *12 May 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,3-8,10,12-14,16,17,19-21,23,25-33,35 and 37-44* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,3-8,10,12-14,16,17,19-21,23,25-33,35 and 37-44* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *6/12/06,5/12/06*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after allowance or after an Office action under *Ex Parte Quayle*, 25 USPQ 74, 453 O.G. 213 (Comm'r Pat. 1935). Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, prosecution in this application has been reopened pursuant to 37 CFR 1.114. Applicant's submission filed on 5/12/06 has been entered. Claims 1, 3-8, 10, 12-14, 16, 17, 19-21, 23, 25-33, 35, 37-44 are pending.

2. The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

Claim Rejections - 35 USC 103

3. Claims 1, 3-6, 8, 10, 12, 14, 16, 17, 19, 21, 23, 25, 27-31, 33, 35, 37, 39-44 are rejected under 35 U.S.C. 103(a) as being unpatentable over Misawa et al (US. PAT. NO. 5,811,837 hereinafter Miasawa) in view of Nakano et al (US. 6,229,513 hereinafter Nakano) and Prak (US. PAT. NO. 4,645,947).

As to claim 1, Fig. 1 of Miasawa discloses a display device comprising a display panel having a TFT (29), a scanning line driving circuit (a gate line driver circuit 21), a signal line driving circuit (a source line driver circuit 12), the signal line driving circuit comprising a plurality of shift registers (a shift register 13 having a plurality of unit cells 210-213). Fig. 11 of Miasawa also disclose a pair of dual clocks signal for driving the shift register having a first

clock signal CL (first signal) and a reversed clock signal CL (second signal) having a different phase from the first clock signal (first signal), and both the clock signal and the reversed clock signal (first signal and second signal) are transmitted to each of the shift register unit cells. Miasawa teaches noise duce to the first and second signals is reduced by the phase difference (col. 12, lines 31-34).

Miasawa does not explicitly disclose the display device having a control circuit for generating the clock signal and a video signal processing circuit. However, Fig. 1 of Nakano teaches a display device having a control circuit (110) connected to a signal line driving circuit for generating display control signals including a clock signal, display data, etc. and transmitting the display control signals to the signal line driving circuit, and a video signal processing circuit (100) connected to the control circuit (110) and the signal line driving circuit (130) for processing a video signal from an external device (180). Thus, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the display device of Miasawa to have the control circuit and the video signal processing circuit as taught by Nakano so as to provide control for the display device and to enhance the resolution of a display panel.

Miasawa as modified by Nakano differs from the claim in that the control circuit does not have a delay circuit for producing the phase difference in the second signal (reversed clock signal) with respect to the phase of the first signal (first clock signal). However, Fig. 1 of Prak teaches a control circuit (clock driver circuit) have a delay circuit (12, 13) for producing the phase difference in the second signal with respect to the phase of the first signal (see Fig. 5). Thus, in order to make and use Miasawa's device with two different phase clock signals, it would have been obvious to one of ordinary skill in the art at the time the invention was made to

modify the control circuit of Miasawa as modified by Nakano to have a delay circuit as taught by Prak since this results in a minimum of skew between a true signal and its complement and results in improved and efficient operation (col. 1, lines 32-36 of Prak).

As to claim 3, Miasawa teaches the first signal and the second signal are clock signals.

As to claims 4, Fig. 11B of Miasawa shows that the first clock signal (CL) has a different rise time period and a different fall time period from the second clock signal (reversed CL).

As to claims 5, Fig. 11B of Miasawa also teaches that a signal rise time period or a signal fall time period of the first or second signal is shorter than a half of a signal holding time period of the first or second signal.

As to claim 6, Fig. 11B of Miasawa shows that the phase difference in the second signal produces a phase difference corresponding to a signal rise time period of the first signal.

As to claims 8, 14, note the discussion of claim 1 above. In addition, Nakano teaches each of the first signal and the second signal is a clock signal. Fig. 11B of Miasawa shows a signal rise time period or a signal fall time period of the first or second signal is shorter than a half of a signal holding time period of the first or second signal.

As to claims 10, 17, Fig. 11B of Miasawa shows that the first clock signal (CL) has a different rise time period and a different signal fall time period from the second clock signal (reversed CL).

As to claims 12, 19, Fig. 11B of Miasawa teaches that a signal rise time period or a signal fall time period of the first or second signal is shorter than a half of a signal holding time period of the first or second signal

As to claim 16, Nakano teaches the first signal and the second signal are clock signals.

As to claim 21, note the discussion of claim 8 above. In addition, Nakano teaches the register latches display data (col. 10, line 5), and Miasawa discloses the first clock signal CL (first signal) and the second clock signal (reversed CL) are input to a same shift register (latch) as claimed

As to claim 23, Fig. 11B of Miasawa shows that the first clock signal (CL) has a different rise time period and a different signal fall time period from the second clock signal (reversed CL).

As to claim 25, Fig. 11B of Miasawa shows that the phase difference in the second signal produces a phase difference corresponding to a signal rise time period of the first signal.

Claims 27 and 33, which are method claims corresponding to the above apparatus claims 1 and 8 are rejected for the same reasons as stated above since such method "steps" are clearly read on by the corresponding "means".

As to claims 28, Miasawa teaches the first signal and the second signal are clock signals.

As to claims 29 and 35, Fig. 11B of Miasawa shows that the first clock signal (CL) has a different rise time period and a different signal fall time period from the second clock signal (reversed CL).

As to claim 30 and 37, Fig. 11B of Miasawa teaches that a signal rise time period or a signal fall time period of the first or second signal is shorter than a half of a signal holding time period of the first or second signal

As to claims 31, Fig. 11B of Miasawa shows that the phase difference in the second signal produces a phase difference corresponding to a signal rise time period of the first signal.

As to claims 39-44, Fig. 5 of Prak shows a length of the phase difference is at least a signal rise time period of the first signal or a signal fall time period of the first signal, and shorter than a half of a signal holding time period.

4. Claims 7, 13, 20, 26, 32, 38 are rejected under 35 U.S.C. 103(a) as being unpatentable over Miasawa, Nakano and Prak as applied to claims 1, 8, 14, 21, 27 and 33 above, and further in view of Shimada (US. PAT. NO. 5,801,678 hereinafter Shimada).

Miasawa as modified by Nakano and Prak teaches the display device including a transmission type LCD panel. Miasawa as modified by Nakano and Prak does not disclose the display device is a projection type display device. However, Fig. 2 of Shimada teaches a LCD display device is a projection type display device having a light source (202) for projection. Thus it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the display device of Miasawa as modified by Nakano and Prak to be a projection type display device as taught by Shimada so as to provide a projection type LCD device for projecting the images on the projection screen.

Conclusion

5. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Uchino (US 6,040,816) teaches active matrix display device with phase adjusted sampling pulses.

6. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Regina Liang whose telephone number is (571) 272-7693. The examiner can normally be reached on Monday-Friday from 8AM to 5:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Richard Hjerpe, can be reached on (571) 272-7691. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Regina Liang
Primary Examiner
Art Unit 2674

6/16/06